GDCQ-xxHH-80CL series

Features

- Compatible with the QSFP28 MSA as describedin SFF-8665
- Optical and host loopback functionality
- Standard CAUI4 electrical interface
- 100Gb/s over 2 wavelengths on a 50GHz DWDM grid enabling 4 Tb/s over a single fiber
- PAM4 modulation format enabling 56Gb/s on a single wavelength
- 80km reach over duplex, SMF
- Adaptive equalization (CTLE) on transmitside electrical input and adjustable output de-emphasis (3 tap FIR filter) to compensate for losses on host
- Typical power consumption of 4.5 W
- Integrated, high-gain FEC encode/decode
- Advanced ADC/DSP receiver technology
- 2-wire management interface with extended digital diagnostic monitoring and alarm functions

Applications

- Data Center Interconnects (DCI)

General

The GIGAC's QSFP28 is a pluggable, DWDM, fiber-optic transceiver for 100 Gigabit Ethernet (100GbE) applications. This module is designed for data center interconnect, which requires highfiber-capacity for links up to 80 km.The optical interface utilizes two, DWDM wavelengths on a 50GHz grid. PAM4 modulation format is used to increase capacity enabling 50Gb/s on each wavelength. Integrated, high-gain FEC (Forward Error Correction) and advanced Rx ADC/DSP technology enable optical reaches up to 80 km over an amplified, DWDM line system. The optical signals are transmitted and received from the module by standard duplex SMF and LC receptacles.

Electrical signals are transmitted and received from the host via a standard, 38-pin connector described in the QSFP28 MSA (SFF-8679). The electrical interface is CAUI-4 compliant (IEEE P802.3bm Annex 83E), splitting the 100Gb/s signals into four, parallel, 25Gb/s NRZ streams.

This module incorporates Inphi's innovative, silicon photonics circuit, arrayed modulation driver, arrayed TIA and advanced DSP technology to provide high performance in a miniature, pluggable package.

Product Selection Guide

DCI modules are designed to operate on a 100 GHz-spaced, DWDM grid in the C-band (ITU-T G694.1, "Spectral girds for WDM applications: DWDM frequency grid"). Each module transmits over two wavelengths spaced at 50 GHz. One lane/wavelength is centered at the 100 GHz ITU grid center + 25 GHz, and the otherlane at ITU grid center – 25 GHz (see table 1 below).

Table 1: Product Selection Guide

CH ID	100 GHz Grid (THz)	Lane 1		Lane 2	
		ITU + 25 GHz (THz)	ITU + 25 GHz (nm)	ITU - 25 GHz (THz)	ITU - 25 GHz (nm)
20	192	192.025	1561.22	191.975	1561.62
21	192.1	192.125	1560.4	192.075	1560.81
22	192.2	192.225	1559.59	192.175	1560
23	192.3	192.325	1558.78	192.275	1559.19
24	192.4	192.425	1557.97	192.375	1558.38
25	192.5	192.525	1557.16	192.475	1557.57
26	192.6	192.625	1556.35	192.575	1556.76
27	192.7	192.725	1555.55	192.675	1555.95
28	192.8	192.825	1554.74	192.775	1555.14
29	192.9	192.925	1553.93	192.875	1554.34
30	193	193.025	1553.13	192.975	1553.53
31	193.1	193.125	1552.32	193.075	1552.73
32	193.2	193.225	1551.52	193.175	1551.92
33	193.3	193.325	1550.72	193.275	1551.12
34	193.4	193.425	1549.92	193.375	1550.32
35	193.5	193.525	1549.11	193.475	1549.52
36	193.6	193.625	1548.31	193.575	1548.71
37	193.7	193.725	1547.52	193.675	1547.92
38	193.8	193.825	1546.72	193.775	1547.12
39	193.9	193.925	1545.92	193.875	1546.32
40	194	194.025	1545.12	193.975	1545.52
41	194.1	194.125	1544.33	194.075	1544.72
42	194.2	194.225	1543.53	194.175	1543.93
43	194.3	194.325	1542.74	194.275	1543.13
44	194.4	194.425	1541.94	194.375	1542.34
45	194.5	194.525	1541.15	194.475	1541.55
46	194.6	194.625	1540.36	194.575	1540.76
47	194.7	194.725	1539.57	194.675	1539.96
48	194.8	194.825	1538.78	194.775	1539.17
49	194.9	194.925	1537.99	194.875	1538.38
50	195	195.025	1537.2	194.975	1537.59
51	195.1	195.125	1536.41	195.075	1536.81
52	195.2	195.225	1535.63	195.175	1536.02
53	195.3	195.325	1534.84	195.275	1535.23
54	195.4	195.425	1534.05	195.375	1534.45
55	195.5	195.525	1533.27	195.475	1533.66
56	195.6	195.625	1532.49	195.575	1532.88
57	195.7	195.725	1531.7	195.675	1532.09
58	195.8	195.825	1530.92	195.775	1531.31
59	195.9	195.925	1530.14	195.875	1530.53

Transceiver Block Diagram

The DCI module integrates transmit and receive functions into a single module as shown in the figure below.

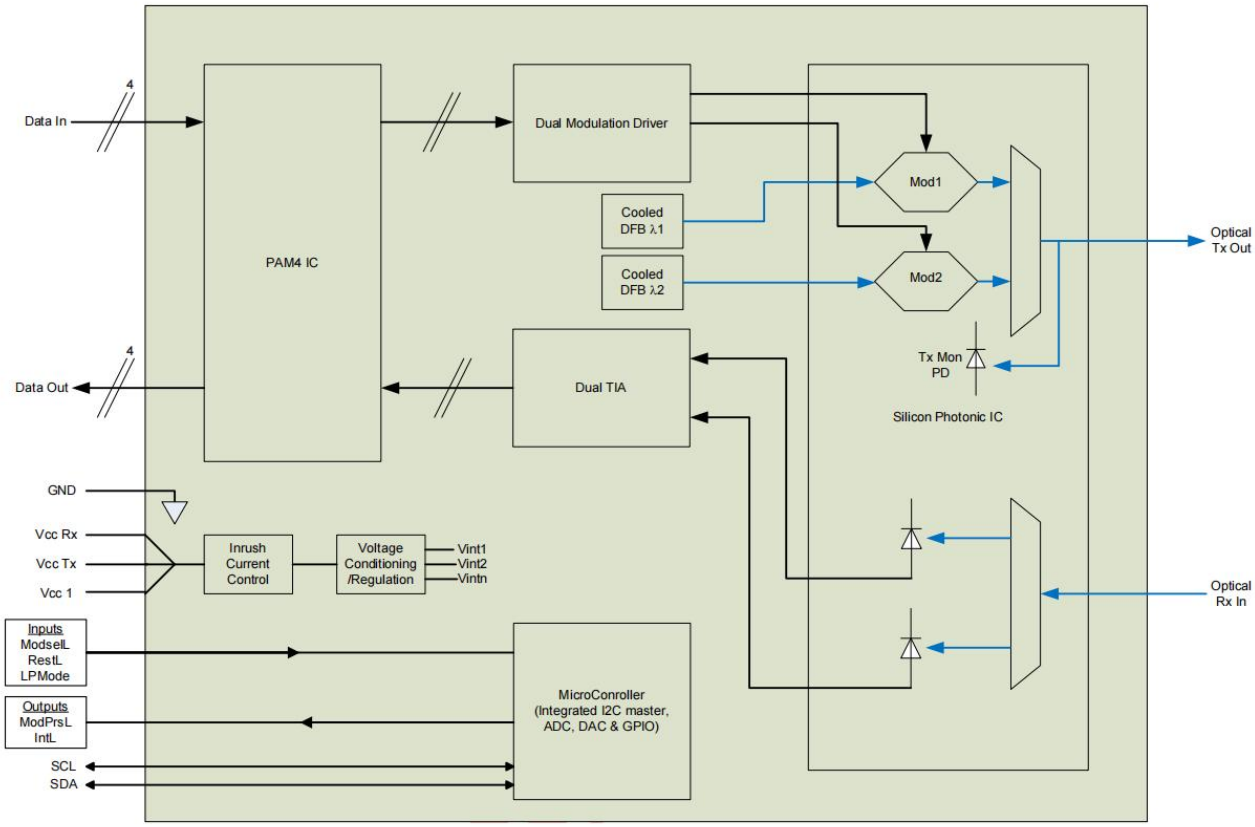


Figure 1 Transceiver Block Diagram

Transmit Path

The transmit path converts four lanes of CAUI-4 (serial NRZ electrical data at a line rate of 25Gb/s) into two wavelengths of PAM4-encoded, DWDM, optical data. The transmitter accepts a 100 Ω differential CML elec- trical signal of up to 900mV peak-to-peak via the standard, 38-pin electrical connector. The data lines are AC- coupled inside the module, so capacitors are not required on the host.

The transmit-side electrical input signals are connected to the receive side of the PAM4 IC. The PAM4 IC offers adaptive input equalization to automatically adjust for host and connector losses. An integrated CDR retimes the data and encodes high-gain FEC onto the data stream. The host FEC must be disabled for the module FEC to be functional.Otherwise, the module must be placed in the internal FEC bypass mode for the host FEC to be operative. The output of the PAM4 IC is connected to a dual-channel, PAM4, modulation- driver IC. The driver IC is used to drive the optical modulators on the Silicon Photonics (SiPho) chip. Optical power is provided by two, CW, cooled, DFB lasers. The laser power is coupled onto the SiPho chip where the individual wavelengths are routed to an optical modulator. The modulated optical signals are then multiplexed onto a single waveguide on the SiPho chip which is coupled to a single fiber that is terminated in a standard, LC receptacle.

Monitors for laser bias, laser output, case temperature, and power supply voltage are provided and results are available through the I2C interface. Alarm thresholds are established for the monitored attributes. Flags are set and interrupts generated when the attributes are outside the thresholds. Flags are also set and interrupts generated for loss of input signal (LOS) and transmitter fault conditions. All flags are latched and will remain set even if the condition initiating the latch clears and operation resumes. All interrupts can be masked and flags are reset by reading the appropriate flag register. Fault detection or channel deactivation through the I2C interface will disable the channel. Status, alarm and fault information is available.

Receive Path

The receiver converts the incoming, DWDM optical signal into four lanes of CAUI-4 compliant electrical signals. The receiver outputs a 100 Ω differential CML electrical signal on the standard, 38-pin electrical con- nector. The data lines are AC-coupled inside the module, so capacitors are not required on the host.

Two wavelengths of PAM4-encoded, DWDM, optical signals are received from a single-mode fiber through a standard LC receptacle. The input fiber is coupled onto the SiPho chip where the optical signal is demulti- plexed into two separate wavelengths/data streams. The individual data streams from the output of the de- multiplexer are routed to an array of two photodiodes on the SiPho chip. The weak electrical signals are amplified in a two-lane, linear, TIA IC. The output of the TIA array is attached to a PAM4 IC where the signal is equalized, timing is recovered, it is digitized by a high-speed ADC and FEC is decoded. The PAM4 IC has adjustable output de-emphasis to equalize loss on the connector and host PCB. Output signals are routed from the DSP to the 38-pin electrical connector for connection to the host.

Monitors for optical input power to the receiver are provided and the results are reported via the I2C interface. Alarm thresholds are established for the monitored attributes. Flags are set and interrupts generated when the attributes are outside the thresholds. Flags are also set and interrupts generated for Loss Of Signal (LOS). All flags are latched and will remain set even if the condition initiating the latch clears and operation resumes. All interrupts can be masked and flags are reset upon reading the appropriate flag register. Status and alarm in- formation are available via the two-wire I2C interface.

Absolute Maximum Ratings

- Stresses beyond those listed here may cause permanent damage to the device.
- These are stress ratings only. Functional operation of the device at these or any other conditions beyond thoseindicated in the “Operating Conditions” and “Electrical Specifications” of this datasheet is not implied.
- Exposure to absolute maximum rating conditions for extended periods may affect device reliability[Note1].

Parameter	Symbol	Conditions	Min	Max	Unit
Storage Temperature[Note2]	Tstore		-40	+85	°C
3.3V Power Supply	Vcc		-0.5	3.6	V
Data Input Voltage, Single-Ended	Vin		-0.5	Vcc+0.5	V
I2C Controls	SDA, SCL		-0.3	3.9	V
ESD: All Pins		HBM	---	1000	V
Storage Humidity[Note2]	RH		5	85	%

Notes:
1. The maximum stress time is 10 second for the absolute maximum ratings of the supply voltage
2. Non-condensing environment

Operating Conditions

Operating conditions specify parameters for which the optical and electrical specifications apply. Optical and electrical characteristics are not defined for operation outside the recommend operating conditions. Reduced reliability or damage to the module may occur for such operation over an extended period of time.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
3.3V Supply Range	Vcc	±5%	3.135	3.3	3.465	V
Power Supply Noise		f = 0 to 5MHz	---	---	50	mVpp
Control Input Voltage High			2	---	Vcc+0.3	V
Control Input Voltage Low			-0.3	---	0.8	V
Rx Diff Data Output Load			---	100	---	Ω
Case Temperature[Note1]	TC	Measured at center of heat sink contact area	20	---	70	℃
Power Dissipation	PD	Tc = 70 °C, Vcc=3.465V, End of Life	---	---	5.0 (MSA class 7)	W
Instantaneous Peak Current at Hot Plug	Icc_ip_8	Instantaneous peak duration < 50 µs	---	---	2000 (MSA class 7)	mA

Notes:
1. The environment in which the module is operated must be controlled to prevent condensation on actively-cooled photonics. Compliance with ambient temperature and humidity limits defined in GR-63 (see Figure 4-1) is required.

Transmitter Optical Characteristics (TP2)

Table 2: Transmitter Optical Characteristics (TP2)

Parameter	Comment	Min	Typ	Max	Unit
Signaling Rate, each lane	Rate = 25.7813Gb/s + FEC OH (~9%) * 2 (PAM4)	Typ -100 ppm	56.25	Typ +100 ppm	Gb/s
Wavelength		See Product Selection Guide			nm
Frequency Control	Frequency control loop used to optimize link performance. Min/max limits indicate control loop range.	λc - 12	---	λc + 12	GHz
Center Wavelength Spacing	Wavelength/lane 1-2 spacing	---	50	---	GHz
Extinction Ratio		---	6	---	dB
Side Mode Suppression Ratio (SMSR)		30	---	---	dB
Average Launch Power, per lane		-11	-10	-8	dBm
Dispersion Tolerance	Residual dispersion (RD) after DCM	-100	---	+100	ps/nm
Average Launch Power of OFF Transmitter, each lane		---	---	-30	dBm
Optical Return Loss Tolerance		---	---	20	dB
Transmitter Reflectance	Defined looking into the transmitter	---	---	-12	dB

Table 3: Receiver Optical Characteristics (TP3)

Parameter	Comment	Min	Typ	Max	Unit
Signaling Rate, each lane	Rate = 25.7813Gb/s + FEC OH (~9%) * 2 (PAM4)	Typ -100 ppm	56.25	Typ +100 ppm	Gb/s
Wavelength		See Product Selection Guide			nm
Damage Threshold[Note1]		10	---	---	dBm
Receiver Power, each lane		-2.0	---	6.0	dBm
Receiver Reflectance		---	---	-20	dB
Required OSNR		31	---	---	dB

Notes:

1.The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal below this average power level.

Receiver Loss of Signal Characteristics (TP3)

Module receiver LOS characteristics are realized by monitoring the DC current of the high-speed photodiodes. Preliminary LOS threshold limits are shown in the table below.

Table 4: Receiver Loss of Signal Characteristics (TP3)

Parameter	Comment	Min	Typ	Max	Unit
LOS asserted threshold - OMA		-10	---	---	dBm
LOS de-asserted threshold - OMA		---	---	-3	dBm
LOS Hysteresis		---	1.0	---	dB

Transmitter Electrical Characteristics (TP1)

For transmitter electrical characteristics, refer to CAUI-4 chip-to-module draft specifications (IEEE P802.3bm Annex 83E). The CAUI-4 host output shall meet the specifications defined below while meas- ured at TP1.

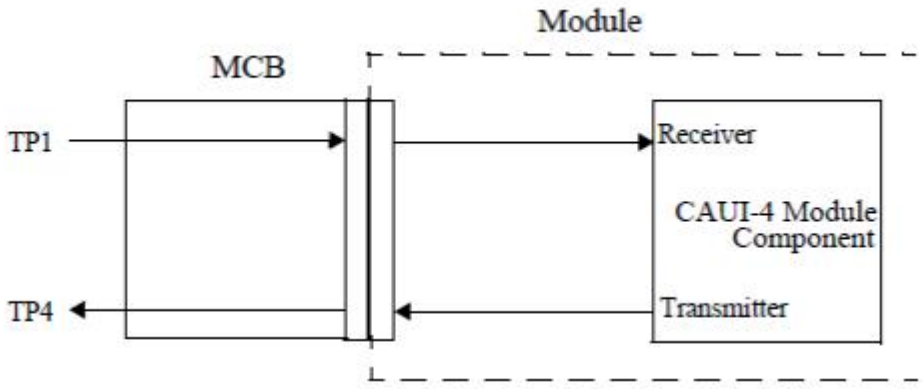


Figure 2 Module CAUI-4 Compliance Test Points

Table 5: Transmitter Electrical Characteristics (TP1)

Parameter	Comment	Min	Typ	Max	Unit
Signaling Rate, each lane		Typ -100ppm	25.7813	Typ +100ppm	Gb/s
DC Common Mode Output Voltage		-350	---	2850	mV
Differential Return Loss	See template[Note1]	---	---	---	dB
Common to Differential Mode Conversion Return Loss	See template[Note2]	---	---	---	dB
Differential Termination Mismatch	At 1 MHz	---	---	10	%

Notes:
1. Reference IEEE P802.3bm Annex 83E, Figure 83E-7 for template
2. Reference IEEE P802.3bm Annex 83E, Figure 83E-8 for template

Receiver Electrical Characteristics (TP4)

For receive electrical characteristics, refer to CAUI-4 chip-to-module draft specifications (IEEE P802.3bm Annex 83E). The CAUI-4 module output shall meet the specifications defined below while measured at TP4 as shown below.

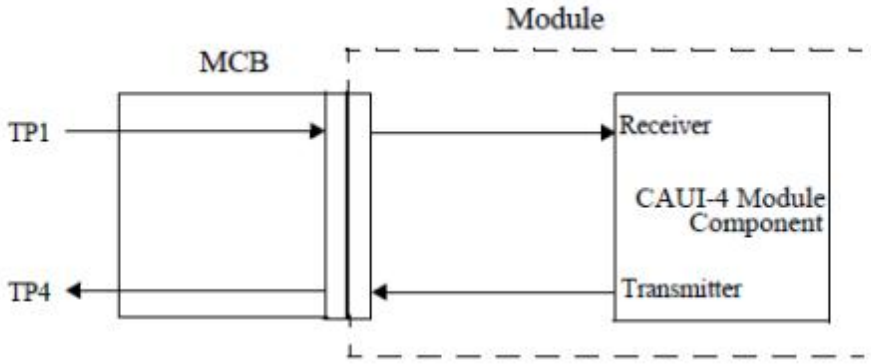


Figure 3 Module CAUI-4 compliance test point

Table 6: Receiver Electrical Characteristics (TP4)

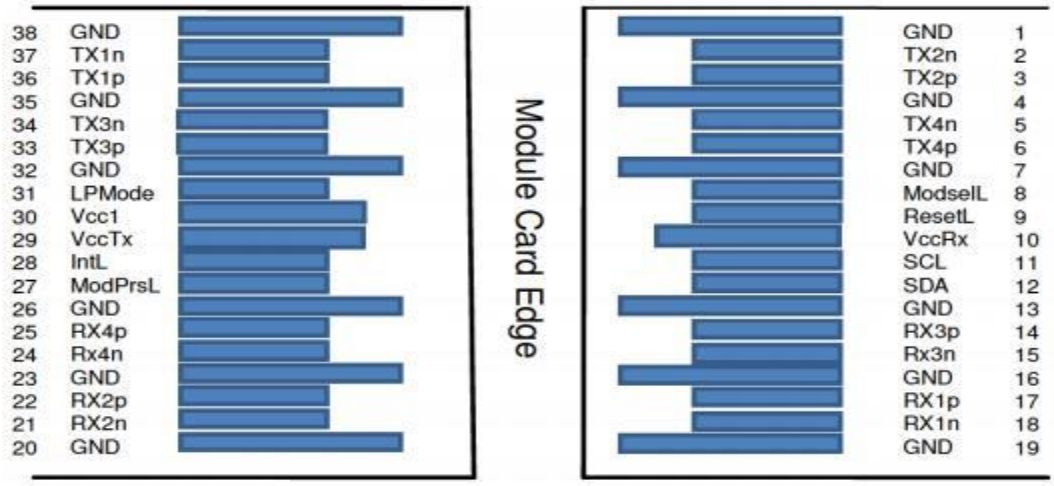
Parameter	Comment	Min	Typ	Max	Unit
Signaling Rate, each lane		Typ - 100 ppm	25.7813	Typ + 100ppm	Gb/s
Common-Mode AC Output Voltage (RMS)		---	---	17.5	mV
Differential pk-pk output voltage swing		---	---	900	mVpp
Eye Width	EW15 at 10-15 probability; PRBS 29-1	0.57	---	---	UI
Eye Height Differential	EH15 at 10-15 probability; PRBS 29-1	228	---	---	mV
Vertical Eye Closure		---	---	5.5	dB
Differential Output Return Loss	See template[Note1]	---	---	---	dB

Common to Differential Mode Conversion Return Loss	See template[Note2]	---	---	---	dB
Differential Termination Mismatch		---	---	10	%
Transition Time (20% to 80%)		12	---	---	ps
DC Common Mode Voltage[Note3]		-350	---	2850	mV

Notes:
1. Reference IEEE P802.3bm Annex 83E, Figure 83E-7 for template
2. Reference IEEE P802.3bm Annex 83E, Figure 83E-8 for template
3. DC common mode voltage is generated by the host. Specification includes effects of ground offset voltage

Electrical Connector

The host side electrical interface is compliant to the QSFP28 MSA (SFF-8679) including pin layout and electrical specifications. See figure below for 38-pin connector layout.



Top Side (Viewed from Top) | Bottom Side (Viewed from Bottom)

Figure 4 38-pin Connection Layout

See table below for pin assignments and descriptions. In standard/default operation, mapping is defined by the MAC and direct CAUI-to-optical-lane mapping does not exist. When the module's FEC is bypassed, CAUI lanes 1 and 2 are mapped to optical lane 1 and CAUI lanes 3 and 4 are mapped to optical lane 2.

Table 7: Pin Assignment

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power supply receiver	2	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Input	3	
15	CML-O	Rx3n	Receiver Inverted Data Input	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Input	3	

18	CML-O	Rx1n	Receiver Inverted Data Input	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Input	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Input	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Input	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Input	3	
26		GND	Ground	1	
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29		Vcc Tx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power Supply	2	2
31	LVTTL-I	LPMode	Low Power Mode	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

Notes:

1. GND is the symbol for signal supply (power) common for the QSFP module. All are common within the QSFP28 module and all module voltages are referenced to this potential unless otherwise noted.Connect these directly to the host board signal-common ground plane

2. Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. The connector pins are each rated for a maximum of 1000 mA

Low-Speed Control Interface

A description of the module control pins can be found below.

ModSelL (LVTTL Input)

ModSelL input node shall be biased to the "High" state in the module. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple modules on a single 2-wire interface bus. When the ModSelL is "high", the module shall not respond to or acknowledge any 2-wire interface communication from the host.

In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any modules are deselected. Similarly, the host shall wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

ResetL (LVTTL Input)

The ResetL pin shall be pulled to Vcc in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by asserting "low" the IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

LPMode (LVTTL Input)

The LPMode pin shall be pulled up to Vcc in the module. The pin is a hardware control used to put modules into a low power mode when high. By using the LPMode pin and a combination of the Power_override, Power_set and High_Power_Class_Enable software control bits (Address A0h, byte 93 bits 0,1,2), the host

controls how much power a module can dissipate.

ModPrsL (LVTTL Output)

ModPrsL is pulled up to Vcc_Host on the host board and grounded in the module. The ModPrsL is asserted "Low" when inserted and deasserted "High" when the module is physically absent from the host connector.

IntL (LVTTL Output)

The IntL pin is an open collector output and shall be pulled to host supply voltage on the host board. When IntL is "low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The INTL pin is deasserted "high" after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of '0' and the flag field is read (see SFF-8636).

Low-speed signaling other than SCL and SDA is based on Low Voltage TTL (LVTTL) operating at Vcc. Vcc refers to the supply voltages VccTx, VccRx, Vcc_host or Vcc1. Hosts shall use a pull-up resistor connected to Vcc_host on each of the 2-wire interface lines (SCL & SDA), and all low speed status outputs.

Table 8: Low-Speed Pin Electrical Specifications

Parameter	Symbol	Condition	Min	Max	Unit
SCL and SDA	VOL	IOL (max)=3.0 mA	0	0.4	V
	VOH		Vcc-0.5	Vcc+0.3	V
SCL and SDA	VIL		-0.3	Vcc*0.3	V
	VIH		Vcc*0.7	Vcc+0.5	V
Capacitance for SCL and SDA I/O pin	Ci		---	14	pF
Total bus capacitive load for SCL and SDA	Cb	3.0 kΩ pull-up resistor, max	---	100	pF
	Cb	1.6 kΩ pull-up resistor, max	---	200	pF
LPMode, Reset and Mod-SelL	VIL	|Iin|<=125 µA for 0V<Vin, Vcc	-0.3	0.8	V
	VIH		2	Vcc+0.3	V
ModPrsL and IntL	VOL	IOL=2.0 mA	0	0.4	V
	VOH		Vcc-0.5	Vcc+0.3	V

Timing of the hardware control functions is specified in SFF-8679 section 8. Where differences exist, the table below takes precedence. The following characteristics are the minimum requirements and are defined over operating conditions unless otherwise noted.

Table 9: Timing for Status and Control Functions

Parameter	Symbol	Comment	Min	Typ	Max	Unit
Initialization Time[Note5]	t_init	Time from power on[Note2], hot plug or rising edge of reset until the module is fully functional[Note3].	---	---	30	s
Reset Init Assert Time	t_reset_init	A Reset is generated by a low level longer than t_reset_init present on the ResetL input.	---	---	2	µs
Serial Bus Hardware Ready Time	t_serial	Time from power on[Note2] until the module responds to data over the two-wire serial bus.	---	---	2000	ms
Monitor Data Ready Time	t_data	Time from power on2 to data not ready, bit 0 of Byte 2, deasserted and IntL asserted.	---	---	2000	ms
Rset Assert Time[Note5]	t_reset	Time from rising edge on the ResetL pin until the module is fully functional[Note3].	---	---	30	s
LPMode Assert Time[Note5]	ton_LPMode	Time from assertion of LPMode (Vin:LPMode = Vih) until module power consumption reaches Power Level [Note1].	---	---	5	s
LPMode Deassert Time[Note5]	toff_LPMode	Time from deassertion of LPMode (Vin:LPMode = Vil) until module is fully functional[Note3].	---	---	30	s
IntL Assert Time[Note5]	Ton_IntL	Time from occurrence of condition triggering	---	---	1	ms

		IntL until Vout:IntL=Vol.				
IntL Deassert Time	toff_IntL	Time from clear on read[Note4] operation of associated flag until Vout:IntL=Voh.This includes deassert times for Rx	---	---	500	µs
Rx LOS Assert Time	ton_los	Time from Rx LOS state to Rx LOS bit set (value = 1b) and IntL asserted.	---	---	100	ms
Tx Fault Assert Time	ton_Txfault	Time from Tx Fault state to Tx Fault bit set (Value = 1b) and IntL asserted.	---	---	N/A	ms
Flag Assert Time	ton_flag	Time from condition triggering flag to associated flag bit set (value =1b)[Note1] and IntL asserted.	---	---	200	ms
Mask Assert Time	ton_mask	Time from mask bit set (Value = 1b)[Note1] until associated IntL assertion is inhibited.	---	---	100	ms
Mask Deassert Time	toff_mask	Time from mask bit (Value = 0b)[Note1] until associated IntL operation resumes.	---	---	100	ms
Application or Rate Select Change Time		Rate Select is not implemented.	---	N/A	---	ms
Power Set Assert Time	ton_Pdown	Time from P_Down bit set (value =1b)[Note1] until module power consumption reaches Power Level 1.	---	---	5	s
Power Set Deassert Time[Note5]	toff_Pdown	Time from P_Down bit cleared (value = 0b)[Note1] until module is fully functional[Note3].	---	---	305	s
ModSelL Setup Time	Host_select_ setup	Setup time on the select lines before start of a host-initiated serial bus sequence.	N/A	---	---	ms
ModSelL Hold Time	Host_select_ hold	Delay from completion of a serial bus sequence to changes of module select status.	10	---	---	µs
Abort Sequence – Bus Release	Deselect _Abort	Delay from a host deasserting ModSelL (at any point in a bus sequence) to the module releasing SCL and SDA.	2	---	---	ms

Notes:

1. Measured from falling clock edge after STOP bit of write transaction.

2. Power on is defined as the instant when supply voltages reach and remain at or above the minimum level.

3. Fully functional is defined as IntL asserted due to DataNotReady, bit 0 byte 2, deasserted. The module should also meet optical and electrical specifications.

4. Measured from falling clock edge after STOP bit of read transaction.

5. Items in red text are not compliant with SFF-8679 which was not written to accommodate cooled, DWDM transmitters.

Timing for Squelch and Disable Functions

Squelch and disable timing is specified in SFF-8679. Where differences exist, the table below takes precedence. The following characteristics are minimum requirements and are defined as over operating conditions unless otherwise noted.

Table 10: Timing for Squelch and Disable Functions

Parameter	Symbol	Comment	Min	Typ	Max	Unit
Rx Squelch Assert Time	ton_Rxsq	Time from loss of Rx input signal until the squelched output condition is reached.	---	---	500	ms
Rx Squelch Deassert Time	toff_Rxsq	Time from resumption of Rx input signals until normal Rx output condition is reached.	---	---	5	s
Tx Squelch Assert Time	ton_Txsq	Time from loss of Tx input signal until the squelched output condition is reached.	---	---	4	s
Tx Squelch Deassert Time	toff_Txsq	Time from resumption of Tx input signals until normal Tx output condition is reached.	---	---	30	s
Tx Disable Assert Time	ton_txdis	Time from Tx Disable bit set (value =1b)1				

		until optical output falls below 10% of nominal.	---	---	2	s
Tx Disable Deassert Time	toff_txdis	Time from Tx disable bit cleared until optical output rises above 90% of nominal (with laser stability).	---	---	30	s
Rx Output Disable Assert Time	ton_rxdis	Time from Rx Output Disable bit set (value = 1b)[Note1] until Rx output falls below 10% of nominal.	---	---	200	ms
Rx Disable Deassert Time	toff_rxdis	Time from Rx Output Disable bit cleared (value = 0b)[Note1] until Rx output rises above 90% of nominal.	---	---	200	ms
Squelch Disable Assert Time	ton_sqdis	This applies to Rx and Tx squelch and is the time from bit set until squelch functionality is enabled.	---	---	N/A	ms
Squelch Disable Deassert Time	toff_sqdis	This applies to Rx and Tx squelch and is the time from bit cleared until squelch functionality is disabled.	---	---	N/A	ms

Notes:
1. Measured from falling clock edge after STOP bit of write transaction.

Timing for SCL, SDA is specified in the common management interface document SFF-8636. Management interface timing parameters are shown in the table below. The following characteristics are minimum requirements and are defined as over operating conditions unless otherwise noted.

Table 11: Two-Wire Interface Timing Parameters

Parameter	Symbol	Conditions	Min	Max	Unit
Clock Frequency	fSCL		0	400	kHz
Clock Pulse Width Low	tLOW		1.3	---	µs
Clock Pulse Width High	tHIGH		0.6	---	µs
Time bus free before new transmission can start	tBUF	Between STOP and START and between ACK and ReStart	20	---	µs
START Hold Time	tHD.STA		0.6	---	µs
START Set-up Time	tSU.STA		0.6	---	µs
Data In Hold Time	tHD.DAT		0	---	µs
Data In Set-up Time	tSU.DAT		0.1	---	µs
Input Rise Time (400 kHz)	tR.400	From (VIL,MAX-0.15) to (VIH, MIN +0.15)	---	300	ns
Input Fall Time (400 kHz)	tF.400	From (VIH,MIN +0.15) to (VIL,MAX - 0.15)	---	300	ns
STOP Set-up Time	tSU.STO		0.6	---	µs
Serial Interface Clock Holdoff (Clock Stretching)	T_clock_hold	Maximum time the slave may hold the SCL line low before continuing with a read or write	---	500	ns
Complete Single or Sequential Write	tWR	Complete (up to) 4-byte write	---	40	ms

Common Memory Map

The memory map is utilized for serial ID, control functions and digital monitoring. Compatible with SFF- 8636 (QSFP28), the memory map is structured as a single address, multiple page approach given as A0xh. This structure permits timely access to addresses in the lower page such as interrupt flags and monitors. Less time critical entries such as serial ID information and threshold settings are available with the page select function. Data used for interrupt handling is located in lower page 00 to enable single block read operations for time critical data. Upper page 01 is not supported. Upper page 02 is supported.

Mechanical Outline

The mechanical outline design of the module as well as the physical PCB layout of the connector should be compliant to SFF-8661, Specification for QSFP28 28Gb/s 4X Pluggable Module. Basic module dimensions are shown below.

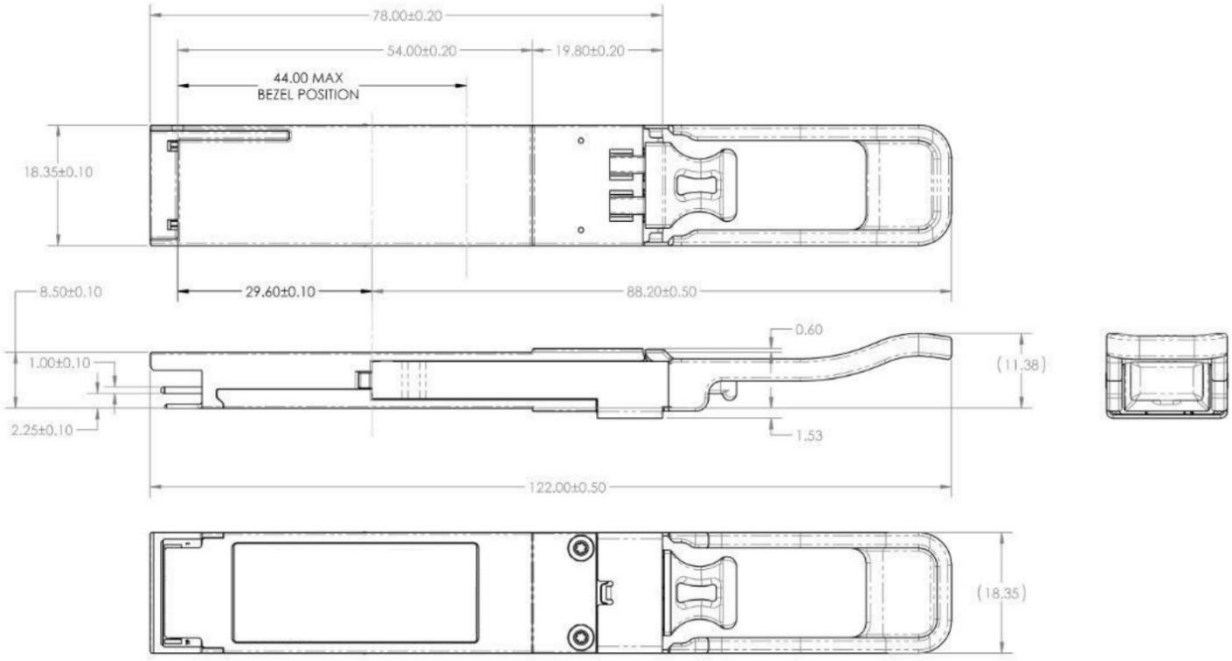


Figure 5 Module Dimensions in mm

ESD Ratings

The transceiver should be handled in an ESD-protected environment utilizing grounded benches, floor mats, ionizers, and wrist straps. It should be shipped in ESD-protective packaging. ESD limit for all pins is 1kV HBM.

Typical of optical transceivers, this module's receiver contains a highly sensitive optical photodetector and transimpedance amplifier which may become temporarily saturated during an ESD strike. This could result in a short burst of bit errors. Such an event might require that the application re-acquire synchronization.

RoHS

The transceiver is lead-free and RoHS 6/6 compliant.

Laser Safety

The transceiver is certified as a Class I laser product per international standard IEC 60825-1:2014 3rd edition and is considered non-hazardous when operated within the limits of this specification. This device complies with 21 CFR 1040.10 except for deviations pursuant to Laser Notice No. 50 dated June 24, 2007.

Caution: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Terms / Definitions / Acronyms

- DWDM: - Dense Wavelength DivisionMultiplexing
- ESD - Electrostatic Discharge
- HBM - Human Body Model

- PAM4 - Pulse Amplitude Modulation with 4 discrete signal levels
- QSFP28 - Quad Small Form factor Pluggable transceiver
- QSFP28 - 28Gb/s QSFP transceiver
- RoHS - Restriction of Hazardous Substances
- SiPho - Silicon Photonics

Applicable Documents

- SFF-8665 QSFP28 28Gb/s 4X Pluggable Transceiver Solution (QSFP28)
- SFF-8636 Specification for Common Management Interface
- SFF-8661 Specification for QSFP28 4X Pluggable Module (mechanical specifications)
- SFF-8679 QSFP28 4X Base Electrical Specification
- IEEE P802.3bm/D2.1 (Feb 2014) Draft standard for Ethernet: physical layer specifications and
- management parameters for 40Gb/s and 100Gb/s operation over fiber optic cables
- ITU-T G694.1 (Feb 2012), Spectral girds for WDM applications: DWDM frequency grid
- JEDEC Human body Model (HBM) JESD22-A114-B for ESD
- Restriction of Hazardous Substances in Electrical and Electronic Equipment, RoHS2 Directive
- 2011/65/EU
- IEC 60825-1 Safety of laser products – Part1: Equipment classification and requirements
- GR-63-CORE (Issue 3, March 2006) – NEBSTM Requirements: Physical Protection

Order Information

Part No.	Description		
GDCQ-xxHH-80CL	DWDM PAM4 QSFP28 100G Ethernet Pluggable Transceiver		
Channel ID (xx= any of the following channels)	**Center Frequency 100 GHz Grid (THz)**	**Channel ID (xx = any of the following channels)**	**Center Frequency 100 GHz Grid (THz)**
20	192.00	40	194.00
21	192.10	41	194.10
22	192.20	42	194.20
23	192.30	43	194.30
24	192.40	44	194.40
25	192.50	45	194.50
26	192.60	46	194.60
27	192.70	47	194.70
28	192.80	48	194.80
29	192.90	49	194.90
30	193.00	50	195.00
31	193.10	51	195.10
32	193.20	52	195.20
33	193.30	53	195.30
34	193.40	54	195.40
35	193.50	55	195.50

36	193.60	56	195.60
37	193.70	57	195.70
38	193.80	58	195.80
39	193.90	59	195.90

Notice

Gigac reserves the right to make changes to or discontinue any optical link product or service identified in this publication, without notice, in order to improve design and/or performance. Applications that are described herein for any of the optical link products are for illustrative purposes only. Gigac makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Revision History

Version	Initiated	Reviewed	Revision History	Release Date
A0	Fei.Han	Smith.Xu	Initialization	2020-06-3

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